UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,233	11/26/2001	Michael A. Nix	X-1012 US	8295

24309 7590 02/27/2004

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,233	NIX, MICHAEL A.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10-12 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-12 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 11/10/03 has been received and entered in the case.

2. Upon further reconsideration, the allowability of claims 17-20 indicated in the last office action is withdrawn based on the rejections discussed below.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "another transistor having a current-handing terminal continuously connected to VSS and a gate connected to the third input terminal" on lines 18-20 causes the claim to be indefinite because it is misdescriptive. As we can seen in Figure 4, the flip-flop including a differential input stage (400, 405) having differential third and fourth input terminals (D, Db). However, the flip-flop does not show, in addition to the differential input stage (400, 405), another transistor having a current handling-terminal continuously connected to VSS and a gate connected to the third input terminal. It appears that the "another transistor" is part of the input stage itself (i.e., it appears that the claim should be inserted the statement --wherein the differential input stage includes-- before "another transistor" on line 18, and changes "f" to --e--). Appropriate correction and/or clarification is requested.

Claims 2-5 is indefinite because it includes the indefinite problem of claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Timoc (USP 6,002,270).

With respect to claim 1, Figure 5 of the Timoc reference discloses a circuit, which includes: a differential input stage (3) having differential first and second input terminals (terminals 40 and 43 receive Y and Y/, see Figure 8 for case X AND Y), differential third and fourth input terminals (terminals 41 and 42 receives X and X/, see Figure 8 for case X AND Y), a first transistor (36), and complementary first and second output terminals (25, 24), wherein the first transistor (36) has a first control terminal connected to the first input terminal (40) and a current-handling terminal directly connected to VSS (ground), and further including another transistor (11) having a first current-handling terminal connected to the first output terminal (25), a second current-handling terminal connected to the second output terminal (24), and a control terminal receiving a clock signal (20)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuki (USP 5,384,493) in view of Choe (USP 6,373,292).

With respect to claim 1, Figure 13 of the Furuki reference discloses a flip-flop circuit includes a first stage (20b) and a second stage (20c), wherein the second stage (20c) includes a differential output stage (3g, 3h) having differential first and second input terminals (OUT1, OUT2) and complementary first and second output terminals (OUT3, OUT4); and a cross coupled circuit (Q37, Q38) having a cross coupled transistor (Q27) configured to continuously receive power from a positive power supply voltage, wherein a gate of the control coupled transistor (Q27) is connected to the second output terminal (OUT4); wherein the first stage (20b) includes a differential input stage (3e-3f) having differential third and fourth input terminals (D, Db) and complementary third and fourth output terminals (OUT1, OUT2) connected to the first and second input terminals (OUT1 and OUT2 of 20b connected to gates of 3g and 3h, respectively, of 20c), respectively, wherein the differential input stage (20b) including another transistor (3e) having a current-handling terminal continuously connected to VSS (ground) and a gate connected to the third input terminal (D); and another cross-coupled circuit (Q35-Q36) including another cross-coupled transistor (Q35) having a gate connected to the fourth output terminal (OUT2). Figure 13 of the Furuki reference does not disclose a transistor having a first current-handling terminal connected to the first output terminal (OUT3), a second current-handling terminal connected to the second output terminal (OUT4), and a control terminal (gate terminal receiving the signal /CLK). However, Figure 2 of the Choe reference discloses a differential circuit which includes a transistor (56 in Figure 2 which is described as transistor 50 in the specification of Choe) having a control terminal (gate) receiving a clock

signal (CLK/), a first current-handling terminal connected to the first output terminal (OUT) and a second current-handling terminal connected to the second output terminal (OUT/) for the purpose of improving the speed of the circuitry (transistor 56 in Figure 2 (described as transistor 50 in the specification) turns on to force the outputs OUT and OUT/ of the circuit approximately half way of power supply VDD, so the voltage swing on the outputs OUT and OUT/ during evaluate phase to go to a logical Lo or Hi is only half the supply voltage VDD, which leads to the advantage of increasing the speed of the circuitry due to the faster switching since the swing of the output is only half of the power supply, see line 25 of Col. 2 to line 10 of Col. 3 of Choe). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the stages (20b and 20c) in the flip-flop circuit (Figure 13) of the Furuki reference with a transistor connected between the outputs of each differential stage (i.e., a transistor connected between nodes OUT1 and OUT2 in the differential stage 20b and its gate receives clock signal CLK because stage 20b is operated with CLKb during evaluate phase, and also another transistor connected between the output nodes OUT3 and OUT4 in the differential stage 20c and its gate receives clock signal CLKb because stage 20c operates with CLK during evaluate phase), as taught by the Choe reference (transistor 56 in Figure 2 of Choe), for the purpose of improving the speed of the circuitry. Thus this modification/combination meets all the limitations of claim 1 because the stage 20c now also includes a transistor having a first current-handling terminal connected to the first output terminal (OUT3), a second current-handling terminal connected to the second output terminal (OUT4), and a control terminal (gate terminal receiving the signal /CLK).

With respect to claim 2, the modification/combination as discussed in claim 1 includes a clock terminal (CLKb) connected to the control terminal (clock terminal CLKb connected to the gate of the transistor connected between the output terminal OUT3 and OUT4).

With respect to claim 3, the above modification/combination shows a second transistor (the transistor connected between terminals OUT1 and OUT2 which having its gate receives clock CLK as discussed above) having a third current-handling terminal connected to the first input terminal (OUT1), a fourth current-handling terminal connected to the second input terminal (OUT2), and a second control terminal (the gate of the transistor connected to receive clock CLK).

With respect to claim 4, the above modification/combination includes a first clock terminal (/CLK) connected to the first-mentioned control terminal (gate of transistor connected between output terminals OUT3 and OUT4 of the stage 20c) and a second clock terminal (CLK) connected to the second control terminal (gate of the transistor connected between the outputs OUT1 and OUT2 of the stage 20b).

With respect to claim 5, the above modification/combination as discussed above meets the limitation that the first and second clock terminals are adapted to receive complementary clock signals.

9. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (USP 5,777,491) in view of Timoc (USP 6,002,270).

With respect to claim 10, Figure 1 of the Hwang et al. reference discloses a circuit, which includes: a differential input stage (11, 12) having differential first and second input terminals (BN, B), differential third and fourth input terminals (AN, A), a first transistor (N3), and

complementary first and second output terminals (Q, QN), wherein the first transistor (N3) has a first control terminal (gate) connected to the first input terminal (BN) and a current handing terminal (source of N3) directly connected to VSS (ground). Figure 1 of the Hwang et al. reference does not disclose that the flip-flop circuit includes another transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a control terminal receiving a clock signal. However, Figure 5 of the Timoc reference discloses a circuit which includes a transistor (11) having a control terminal (gate) receiving a clock signal, a first current-handling terminal connected to the first output terminal (25) and a second current-handling terminal connected to the second output terminal (24) for the purpose of improving the speed of the circuitry (during the equalization phase, outputs 25 and 24 are forced to a voltage which equals approximately half of the power supply voltage Vdd, so the outputs 25 and 24 swing to logical Lo or Hi during the evaluate phase is only half the supply voltage VDD, which leads to the advantage of increasing the speed of the circuitry due to the faster switching since the swing of the output is only half of the power supply, see lines 1-30 of Col. 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit (Figure 1) of the Hwang et al. reference with a transistor connected between the outputs of the circuit (i.e., a transistor connected between nodes Q and QN), as taught by the Timoc reference (transistor 11 in Figure 5 of Timoc), for the purpose of improving the speed of the circuitry. Thus, all of the limitations in claim 10 are met.

With respect to claim 11, Figure 1 of the Hwang et al. reference shows that the input stage (11, 12) includes a first leg (12) including the first transistor (N3) and a second transistor

(N4) connected in parallel, the second transistor (N4) having a second control terminal (gate) connected to the third input terminal (AN).

With respect to claim 12, Figure 1 of the Hwang et al. reference shows that the input stage (11, 12) includes a second leg (12) having third and fourth transistors (N2, N1) connected in series, the third transistor (N2) having a third control signal (gate) connected to the second input terminal (B) and the fourth transistor (N1) having a fourth control terminal (gate) connected to the fourth input terminal (A).

10. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choe (USP 6,373,292) in view of Hwang et al. (USP 5,777,491), and further also in view of Timoc (USP 6,002,270).

With respect to claim 15, Figure 2 of the Choe reference discloses a circuit (40) which includes an output stage (40), wherein the output stage (40) receiving a differential input signal (In, In/). Figure 2 of the Choe reference does not specially disclose how the differential input signal (In, In/) is generated. However, Figure 1 of the Hwang et al. reference discloses an input stage circuit that generate differential signal (Q, QN) for the purpose of low power dissipation and requires only a small chip area for fabrication (see Col. 2, lines 1-8 of the Hwang et al. reference). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the circuit in Figure 1 of the Hwang et al. reference to provide the differential signal (Q, QN) to the differential input (In, In/) of the circuit in Figure 2 of the Choe reference (i.e., signals Q and QN in Figure 1 of the Hwang et al. reference are respectively to signals In and In/ in Figure 2 of the Choe et al. reference) for the purpose of low power dissipation and requires only a small chip area for fabrication (see Col. 2, lines 1-8 of the Hwang

et al. reference). Note that this combination meets all the limitation of this claim 15 except for the differential input stage (Figure 1 of the Hwang et al. reference) also includes another transistor having a first current-handling terminal connected to the first output terminal of the differential input stage, a second current-handling terminal connected to the second output terminal of the differential input stage, and a control terminal receiving a clock signal. However, Figure 5 of the Timoc reference discloses a circuit which includes a transistor (11) having a control terminal (gate) receiving a clock signal, a first current-handling terminal connected to the first output terminal (25) and a second current-handling terminal connected to the second output terminal (24) for the purpose of improving the speed of the circuitry (during the equalization phase, outputs 25 and 24 are forced to a voltage which equals approximately half of the power supply voltage Vdd, so the outputs 25 and 24 swing to logical Lo or Hi during the evaluate phase is only half the supply voltage VDD, which leads to the advantage of increasing the speed of the circuitry due to the faster switching since the swing of the output is only half of the power supply, see lines 1-30 of Col. 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit (Figure 1) of the Hwang et al. reference with a transistor connected between the outputs of the circuit (i.e., a transistor connected between nodes Q and QN), as taught by the Timoc reference (transistor 11 in Figure 5 of Timoc), for the purpose of improving the speed of the circuitry. Thus, all of the limitations in claim 10 are met. Thus, this combination/modification meets all the limitation of claim 15, i.e., the above combination/modification includes an input stage (Figure 1 of the Hwang et al. reference) including a differential input stage (11, 12) having differential first and second input terminals (BN, B), differential third and fourth input terminals (AN, A), a first transistor (N3),

and complementary first and second output terminals (Q, QN), wherein the first transistor (N3) has a first control terminal (gate) connected to the first input terminal (BN) and a current handing terminal (source of N3) directly connected to VSS (ground), and another transistor (as discussed in the modification discussed as similar to claim 10) having a first current-handling terminal connected to the first output terminal of the differential input stage, a second current-handling terminal connected to the second output terminal of the differential input stage, and a control terminal receiving a clock signal; an output stage (Figure 2 of the Choe reference) including differential fifth and sixth input terminals (In and In/, Figure 2 of Choe) connected to respective ones of the first and second output terminals (Q and QN of Hwang et al.), complementary third and fourth output terminals (OUT and OUT/ in Figure 2 of Choe), and a transistor (56, Figure 2 of Choe) having a second control terminal (gate), a first current-handling terminal (64, Figure 2 of Choe) connected to the third output terminal (OUT, Figure 2 of Choe) and a second current-handling terminal (62, Figure 2 of Choe) connected to the fourth output terminal (OUT/, Figure 2 of Choe).

With respect to claim 16, Figure 2 of the Choe reference in the above combination also meets the limitation of a clock terminal (CLK/) connected to the second control terminal (gate of transistor 56 in Figure 2 of Choe).

11. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuki (USP 5,384,493) in view of Choe (USP 6,373,292), as discussed in claim 1 above, and further in view of Tung et al. (US 2003/0052720 A1).

With respect to claim 17, the above combination/modification as discussed in claim 1 above discloses a flip-flop circuit except for specifically that the flip-flop circuit is in a counter.

However, Figure 2A of the Tung et al. reference teaches that, a divide-by-2 counter is made by cascading two D-flip-flop together with the outputs of the second D-flip-flop feedback to the inputs of the first D-flip-flop (see Figure 2A and paragraph [0026] on page 3 of the specification of Tung et al.). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to cascade two D-flip-flops (wherein each flip-flop is the circuit discussed in the above combination/modification of Furuki vs. Choe as discussed in claim 1) together with proper feedback connections (i.e., a first flip-flop having outputs connected to the D inputs of the second flip-flop, and the outputs of the second flip-flop are connected to the D inputs of the first flip-flop) for the purpose of making a divide-by-two counter. Therefore, this combination/modification meets all the limitation of claim 17, as the counter includes: a first flip-flop (the first flip-flop in the divide-by-two counter which is the modification/combination of Figure 13 of Furuki in view of Figure 2 of Choe as discussed in claim 1 above) having: a differential output stage (20c in Figure 13 of Furuki) having differential first and second input terminals (OUT1, OUT2 in Figure 13 of Furuki) and complementary first and second output terminals (OUT3, OUT4 in Figure 13 of Furuki); and a first transistor (transistor 56 in Figure 2 of Choe) having a current-handling terminal connected to the first output terminal (transistor 56 in Figure 2 of Choe connected between the outputs OUT3 and OUT4 in Figure 13 of Furuki as discussed in claim 1 above), a second current-handling terminal connected to the second output terminal (transistor 56 in Figure 2 of Choe connected between the outputs OUT3 and OUT4 in Figure 13 of Furuki as discussed in claim 1 above), and a first control terminal (gate receiving clock signal CLKb as discussed in claim 1); and a cross coupled circuit (Q37, Q38) having a cross coupled transistor (Q37) directly connected to a positive power supply voltage, wherein a

gate of the cross coupled transistor (Q37) is connected to the second output terminal (OUT4); and a second flip-flop (the second flip-flop in the divide-by-two counter which is the modification/combination of Figure 13 of Furuki in view of Figure 2 of Choe as discussed in claim 1 above) having: a differential input stage (20b in Figure 13 of Furuki) having a differential third and fourth input terminals (D, Db in Figure 13 of Furuki) connected to the respective first and second output terminals of the first flip-flop (the outputs of the first flip-flop connected to the inputs of the second flip-flop for making a counter as discussed above), a second transistor (3e), and complementary third and fourth output terminals (OUT1, OUT2), the second transistor (3e) having a gate connected to the third input terminal (D) and a current handling terminal directly connected to VSS (ground); and a third transistor (transistor 56 in Figure 2 of Choe as discussed in claim 1) having a third current handling terminal connected to the third output terminal, a fourth current handling terminal connected to the fourth output terminal (transistor 56 in Figure 2 of Choe connected between the outputs OUT3 and OUT4 in Figure 13 of Furuki as discussed in claim 1 above), and a second control terminal (gate receiving clock signal CLK as discussed in claim 1).

With respect to claim 18, the first and second control terminals are adapted to receive complementary clock signals (the gate of the first transistor and the gate of the third transistor receiving clock signals CLKb and CLK, respectively as discussed above).

With respect to claim 19, it is seen in the above modification/combination that the first flip-flop (first flip-flop of the divide-by-two counter, wherein the flip-flop is discussed as in claim 1 above) includes a second differential input stage (20b, Figure 13 of Furuki) having differential fifth and sixth input terminals (D, Db in Figure 13 of Furuki) and complementary

fifth and sixth output terminals (OUT1 and OUT2 in Figure 13 of Furuki), wherein the fifth and sixth output terminals are connected to the first and second input terminals (OUT1 and OUT2 in Figure 13 of Furuki connected to inputs of 20c).

With respect to claim 20, it is seen in the above modification/combination that the second flip-flop (second flip-flop of the divide-by-two counter, wherein the flip-flop is discussed as in claim 1 above) includes a second differential output stage (20c, Figure 13 of Furuki) having differential fifth and sixth input terminals (OUT1, OUT2 in Figure 13 of Furuki) connected to the third and fourth output terminals (outputs OUT1 and OUT2 of input stage 20b connected to the inputs of output stage 20c in Figure 13 of Furuki).

Response to Arguments

12. Applicant's arguments filed on 11/10/03 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

LN
Date: February 7, 2004

Long Nguyen
Art Unit: 2816